STRATEGIES TO DECREASE POWER AND PROPAGATION DELAY IN CMOS TAPERED BUFFER: A REVIEW

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Abstract: A CMOS Tapered buffer is used to increase the driving ability of the logic circuitry whenever it is connected with large capacitive load. The increasing width of each inverter in the chain of CMOS inverters is based on tapering factor. The scaling or tapering factor of each stage is dependent on technology used, driving load and the number of stages used. Buffer Insertion is a very effective approach for delay reduction. But in every new generation deep submicron technology, buffer insertion is becoming a major problem, because of their number of stages and also because they now a major source of power dissipation. Hence a trade-off is required between delay and power consumed. Thus there is a need for a new approach that while reducing the delay, also consumes less power. In this paper different strategies are presented which can be attractive in the design of buffer circuits.

Keywords: Average power dissipation, CMOS inverter, Output capacitive load, Tapering factor

Introduction: The chain of cascaded CMOS inverters is used to drive large capacitive loads with amplifying ability. With advances in the VLSI (Very Large Scale Integrated) technology, the use of inverting or non – inverting buffers is used to drive large capacitive load so that cascaded tapered inverters can deliver large current for fast response. The size of NMOS and PMOS in each stage of inverter chain is dependent on the optimized scaling factor for minimum delay. The fixed optimized tapered factor used in each stage results in equal rise and fall time and delay for each stage [1].

High performance and low power dissipation VLSI design is the attractive feature in portable systems. Thus less power dissipation in buffer circuit demands a decrease in both V_{dd} and $V_{th}$to sustain propagation delay, but decrease in V_{th} increases leakage power and short circuit power exponentially. Similarly reducing C_L and increasing W/L ratio of the transistor for minimizing delay may increase self loading and output capacitance [2]. So this allows tradeoff between different parameters for both power and delay and the most preferred techniques used for the design of Tapered buffer are represented in this paper. The first order analysis

This paper discusses the Basic design of a CMOS tapered buffer in section II, after that section III shows different strategies for the design of High speed and Low power tapered buffer and section IV concludes this paper.

Design of a CMOS Tapered Buffer: In CMOS integrated circuits, large capacitive loads are often present. In order to drive large capacitive loads with current amplifying ability Tapered buffers are used. Buffers are used for the purpose of signal restoration and delay reduction. Since propagation delay is dependent on output capacitive load (C_L) and "ON resistance" (R_P or R_N) of NMOS and PMOS respectively. It is possible to approximate the transient response of a CMOS inverter to a RC model and the propagation delay for an instantaneous input transition is given as (R_P . C_L)or (R_n . C_L). Thus, buffer circuits are required which can drive the load at high speed while not degrading the performance of previous stages [3]. The output of inverting or non - inverting tapered buffer is generally connected between Logic circuit and Capacitive load to drive large current or amplifying current.

The structure of CMOS tapered buffer was first presented by Lin and Linholm in 1975 [2].This structure was consists of a chain of inverters where each transistor channel width is F (tapering factor) times larger than that of the previous stage inverter. This tapering factor is strongly process dependant means it's all parameters determined by the process [4]. For each stage, the ratio of output current drive and output capacitance remains constant which results in equal rise, fall and delay times for each stage. Split-capacitor model is used of a tapered buffer in Figure 1, as given by Li, Haviland and Tuszynski [5].

The given figure shows cascaded CMOS Tapered inverters with capacitance expressions at the output of each stage.

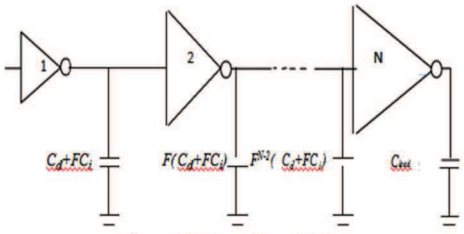

Figure 1: N stage Taper buffer.

The number of stages required in buffer design depends on technology dependant factor F, load capacitance (C_L) and input capacitance (C_g) of first inverter in the buffer chain. Its expression was

derived in [5, 10] is given below

$N_D = \frac{ln(C_L/C_g)}{ln(F)}$

Where N_D represents the no of stages required in the design of tapered buffer to achieve minimum delay and F is technology dependant tapering factor.

The value of propagation delay can be calculated using [1, 5] for tapered buffer having N number of stages is given as

$$T_{delay} = NV_{DD}\frac{C_d + FC_g}{I_{DO}}\left(\left(1.125\frac{V_{DO}}{0.8\,V_{DO}}\,ln\left(\frac{10\,V_{DO}}{e\,V_{DO}}\right)\right)\left(\frac{1}{2} - \frac{1-vt}{1+\alpha}\right) + \frac{1}{2}\right)$$

Where V_{DD} is applied D.C voltage to buffer circuit which is based on technology node, α is velocity saturation index and $vt = V_{th} / V_{DD}$.

The parameters C_g and C_d (gate and drain capacitance of minimum sized inverter in tapered buffer chain)depend upon the layout and fabrication technology used for the tapered buffer design. However, for a given technology and buffer layout, these values are considered to be constant. Therefore, the design of a tapered buffer reduces to choosing N, and then F, based on a specific load capacitance [1].

The values of V_{DO} and I_{DO}(Drain saturation voltage and current at $V_{GS} = V_{DD}$)can be approximated using the alpha power model, and both were derived in [8].

The total power dissipation in a CMOS tapered buffer is given as following expression

$P_T = P_{dyn} + P_{S.C} + P_{sub}$

Analytical expressions for the short circuit power dissipation, dynamic power and sub- threshold power dissipation are described using [1,4] and are given as

(a) $P_{dyn} = V^2_{DD} f (Cd + FC_g) \left[\frac{(C_L/C_g - 1)}{(F - 1)}\right]$

where f is the frequency of operation

(b)$P_{S.C} =$

$$P_{dyn}\left(9/8 + \frac{V_{DO}}{0.8\,V_{DD}}\,ln\,\frac{10}{V_{DD}}\right)\frac{1}{\alpha-1}\frac{1}{2^{\alpha-1}}\frac{(1-2V_T)^{(\alpha+1)}}{(1-V_T)^{\alpha}}$$

here V_{DO} is the drain saturation voltage at $V_{GS} = V_{DD}$ and α is velocity saturation index

(c)$P_{sub} = V_{DD}\, I_{SUB}\left[\frac{(C_L - 1)}{(F - 1)}\right]$ Where I_{SUB} is the sub-threshold leakage current its value can be approximated using simulation tool or analytically.

The three power components of the total power nearly attributed to the average power dissipation of a CMOS tapered buffer circuit.

Different Allowable Strategies: The basic design step of a CMOS Tapered buffer is to place it between the logic circuit and driving load.Different strategies which were developed by different researchers for the design of optimized Tapered buffer in terms of power and speed of operation are listed as below:

Optimum Threshold voltage: The input signal to buffer chain can be made to rise / fall faster by keeping the voltage threshold to be lower for fast signal switching. The ratio of load capacitance (C_L) and gate capacitance of first inverter (C_g) in CMOS tapered buffer helps to decide tapering factor first and then the number of stages N required for implementing the required logic. Weighing factors (ka and k_b) can be approximated as [5]. The strategy which includes the effect of power dissipation in buffer design is to have Cost Function (C.F), defined as

$C.F = P^{k_a} \times T^{k_b}$

Where k_a is the power dissipation weighing factor and k_b is the propagation delay weighing factor exponent.

Given expression that gives the optimum value of threshold voltage for minimized power delay product is the function of arbitrary number of stages N and can be derived analytically[10].

$V_{th_{opt}} = (0.35 - 0.07\frac{N - N_{opt} - 1}{N_D - N_{opt}})\,(1 + \ln(\frac{k_a}{2k_b}))$

Where $N_{opt} = [N_D\{1 - e^{-0.7(ka/kb)}\} - 1]$ and N_D represents the number of stages in the buffer chain to achieve minimum delay irrespective of power dissipation.

Thus after calculating the optimum number of stages N_{opt} and substituting this value in above expression for finding $V_{th_{opt}}$ yields minimum of Cost Function.

Switching Threshold Voltage range: To set the value of V_{th} in the range of (0.2 V_{DD} – 0.4 V_{DD}) optimizes both the power dissipation and delay. Increasing the threshold between 0.2 V_{DD} and 0.4 V_{DD} gives the significant reduction in power with minimal delay penalty due to decease in sub threshold leakage current with increase in threshold beyond 0.2 V_{DD} [12]. The CMOS circuit design restricts the threshold voltage beyond 0.4 V_{DD} because for symmetrical Voltage transfer characteristics of a CMOS inverter, V_{th} should be less than switching threshold V_M = 0.5 V_{DD} for higher noise margins and reduced noise glitches. Reduced noise glitches result in lesser power consumption and hence help in reducing the total power consumed.

Multi–Threshold voltages: The total power dissipation in CMOS circuits is very sensitive to the threshold voltage variations rather the propagation delay, especially close to the V_{th} = 0.2 V_{DD} point [7].It has been researched that the existence of dual threshold voltage in CMOS inverter circuits helps in avoiding cross-talk in buses providing the noise falls in threshold interval. The penalty in delay due to use of low threshold value can be compensated by increasing the number of stages in buffer design. Thus, an overall saving on power dissipation and propagation delay of cascaded inverters can be achieved.

Optimum Tapering factor: To meet the current carrying ability, the size of NMOS/PMOS in each

stage of CMOS Tapered buffer is increased by the tapering or scaling factor which is dependent on the ratio of capacitive load and gate capacitance of minimum sized inverter in the inverter chain.

The value of Optimum tapering factor is slightly different from the value of classical tapering factor (e = 2.72) or a value which is more in line with FO4 (fan out of 4) delay, because the value of delay or power weighing factors make it more convenient for low power or fast speed buffer. But it was deduced from the previous research that the delay dependence on the tapering factor is rather weak. Not much speed is lost even if the tapering factor is doubled from, that is, four to eight [3]. The delay increase is only 20%.But its value plays an important role for deciding the Buffer area and it is technology dependant factor also. For simplicity area of each inverter in the tapered buffer is assumed to be proportional to its size as determined by tapering factor. So the tradeoff between the delay and buffer area restrict the selection of the tapering factor. The Most convenient solution of the optimum tapering factor using following expression may result for the optimized speed and lesser area utilization of the buffer circuit [12].

$$F_{opt} = \left(\frac{C_L}{C_g}\right)^{\frac{1}{N_{opt}}}$$

Where $N_{opt} = [N_D \{1 - e^{-0.7\left(\frac{k_a}{k_b}\right)}\} - 1]$ and N_D represents the optimum number of stages used and k_a and k_b are power and propagation delay weighing factors.

If the value of optimum tapering factor (F_{opt}) is known then optimum number of stages in the design of Tapered buffer can be found using above expression for the optimum speed of operation of a CMOS buffer.

Choice of Non uniform or Variable Tapering factor: The dependence of delay penalty factor with capacitive loads was studied by many researchers since it was found that for each large capacitive load there are a certain number of stages of inverters for the design of Tapered buffer. Therefore, in medium fan-outs circuits where ($C_L < 50\ C_g$) which require one or two staged buffer, an FT (fixed or uniform tapered) buffer model results in better designs. But for large driving loads like off-chip circuitry and clock drivers, a VT (variable or non uniform tapered) buffer results in more compact layouts (significant area saving) for comparable delay penalties. The delay of this buffer and expression for variable tapering factor is given in [6].

Technology selection: Proper technology selection is one of the key aspects of power management in the design of CMOS buffer since capacitance per node reduces by 30%. Process designers scale both the applied voltage and the oxide thickness, however as the voltage gets smaller, the threshold voltage also scale down to meet the performance targets in that technology. Voltage scaling increases the sub threshold current and hence the leakage power. National Technology Roadmap for Semiconductors reflects the technology shrinkage of gate delay of 0.7 per generation and a corresponding doubling of clock frequency every two generations [13]. This speeds up the chip performance but doubles the power dissipation of MOSFET's used in CMOS inverters circuits. Thus the sizing of transistors which is based on technology dependant tapering factor in buffer design should be such that it can fix Vth and frequency of operation for optimized power dissipation at load.

Use of minimum sized Feedback network at last stage of a Tapered buffer: Minimum sized Inverter feedback circuit connected between the last stage of a tapered buffer circuit and capacitive load minimizes the short circuit power dissipation. Since the feedback circuitry delays the charging and discharging time at gate terminals of NMOS and PMOS transistors of last stage inverter. Thus this strategy may avoid the transistors used in last stage being on at the same time and thus reduces the short circuit power in buffer circuit. But the overall delay of this tapered buffer increased slightly due to use of more transistors [12].

Choice of transition times of the Input and output signals: The short-circuit power dissipation is a function of both the output load capacitance as well as the transition time of input signal [4].A good index that takes care of both of these parameters is the output transition time of the signal.

(1) In FT (fixed tapering) buffers, the input transition times are almost equal to output transition times at each stage because of similar relative loading from one stage to other stage assuming that ratios of PMOS and NMOS transistors resulting in symmetrical rise and fall times.

(2) In VT (variable tapering) buffers, the input transition time can be made less than to output transition times at any stage. Thus ratio of short circuit power dissipation to dynamic power dissipation of VT buffer is less than that of FT buffer [6].

Buffer based on CNFET(Carbon Nanotube FET) technology: This recent design scheme not only reduces minimizes short circuit and leakage power but also optimizes the propagation delay. In Carbon Nanotube Field Effect Transistors (CNFETs) one or more semiconducting SWCNT's (Single Wall Carbon Nanotube FET's) are used as the channel of the device [14].Potassium doped source and drain CNT which can be used in the design of tapered buffer with unipolar characteristics is called MOSFET-like

CNFET. The advantage of using CNFET is that its threshold voltage can be adjusted by changing the diameter of its CNT's. This practical characteristic makes CNFET more flexible than MOSFET for designing many digital circuits and very suitable for designing recent multi-threshold circuits.

In this technology, the total size of the CNFET is determined by the width of the gate. Further the gate width can be determined by the pitch. By setting the minimum gate width Wmin and the number of tubes N, the gate width can be approximated as [11].

minWg= Max(W , N *Pitch)

Where, Wgmin is the minimum width of the gate and N is the number of Nanotube under the gate.

Moreover, it was observed in the previous research work that the current-voltage (I-V) characteristics of the MOSFET and CNFET devices are alike and characteristics of the CNFET also has a symmetrical shape at a 1 to 1 (pFET : nFET) ratio. To design a circuit with best performance based on an average power consumption and speed, it is very important to determine the threshold voltages of N-CNFET and P-CNFET because this affects the switching speed, the current driving capability and leakage power. Similar to a MOSFET device, a CNFET has also threshold voltage which is the voltage required for turning on any switching device through the gate.

In CNFET technology, the gate capacitance depends on the number of tubes and the pitch (where the pitch is defined as the distance between the centres of two adjacent CNTs in the same device [14]). By analyzing the device characteristics of a CNFET, performance parameters such as high speed, low power and low area overhead can be achieved when designing circuits using this technology.

CMOS tapered buffer using sleep transistors technique: This method provides very high reduction in static power during periods of inactivity or sleep state of NMOS and PMOS in CMOS inverter. However the output states during active mode of operation will not be at good logic1 and logic 0 values. To obtain good logic output levels during active mode of operation and to achieve the retention of previous output state, state retention transistors can be used across the sleep control transistors [13].

During standby mode of operation the sleep signals, the different control logic level used in its circuit design causes the PMOS and NMOS transistors in the power gating circuit to be switched off and provide lower leakage current flow through the off transistors. The state retention can be achieved by making both of the sleep control signals 0 or 1[11].

This Technique can be utilized in those situations which do not demand good output voltage levels. The state retention inverter can result in good leakage and dynamic power reduction as well as the previous output state can be retained using single Vth transistors only.

Conclusion: In our paper, different strategies for the design CMOS tapered buffer which is driving large load were discussed. These different approaches can lead to the selection of choice of parameters for the circuit of Tapered buffer. Unfortunately designing for low power adds another dimension to the already complex design problem and design has to be optimized for performance, power as well as area utilization. It can be observed from the above description that by increasing the threshold voltage of NMOS or PMOS within ($0.2\ V_{DD} - 0.4V_{DD}$) range, sub threshold power can be reduced to reduce total power dissipation. Hence, the above discussed design strategies can be helpful to provide power efficient scheme for portable VLSI systems where multi V_{dd}supply is used to drive different sub sections to save power for logic blocks. Since the switching activity of an inverter is not so much varying because same logic topology used in the design of buffer and fixed tapered factor which describes the average capacitance charge during each cycle of clock pulse minimizes the power dissipation. The multistage CMOS inverters based on the above mentioned strategies can be the choice of low power circuits with low delay penalty. Finally, we can say that Optimum values of Tapering factor and number of stages of inverters in the buffer chain may be the primary choices and challenging issue for the design of Tapered buffer with high driving capability.

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Tabular representation of different Allowable strategies for Buffer designing: Table-1 summarizes and compares the key matrices of the different strategies that were discussed above in this paper for the design of low power fast switching Tapered buffer.

Table-1

Key parameters for the Buffer Design	**Strategy of Design Scheme and used technology**	**Trade off parameters**	**Delay saving (in %)**	**Power saving (in %)**
Fixed Tapering Factor	Feedback network Tapered buffer when N = N_D and Fixed scaling factor(F) in 70nm	Propagation delay and power dissipation (It uses more number of transistors)	Increased (about 2 %)	Average power Decreased (about 15%)
Variable Tapering factor	CMOS variable Tapered buffer with high capacitive loads(50 C_g – 10000C_g)	Number of stages and choice of variable scaling Factor	Longer Delay (about 2%)	Short circuit power Decreased (about 10% for more no. of stages) and Lesser Area utilization
Single V_{th} transistor	Novel Sleep Inverter based buffer in 90nm	Lower output logic levels	Same delay as compared to earlier sleepy keeper technique	Total power decreased by (a factor of X 3.5)
Variable V_{th}Transistors	CMOS tapered Buffer based on F_{opt} and $N_{opt}$with varying capacitive load in 65nm	As $k_a$increases, it becomes crucial to allow $V_{th}$to vary	Increased (about 30 %)	Decreased (about 70%)

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